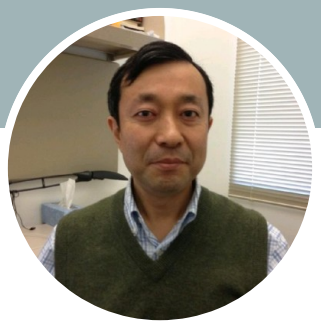
Exhibit I



Yukio Otaguro

Hardware Engineer

San Jose, California, United States · Contact info

128 connections

Message More

About

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Activity

128 followers

Yukio hasn't posted lately

Yukio's recent posts and comments will be displayed here.

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Experience

Hadware Engineer

Oracle

Feb 2010 - Aug 2017 · 7 yrs 7 mos

santa clara, CA

Standard cell library design.
CPU integration. Global clock, power grid, bump, design and physical verification.

Hardware Engineer
Sun Microsystems
May 2001 - Jan 2010 · 8 yrs 9 mos
Santa clara ca

CPU integration. Floorplan, pin assignment, abstract management, routing, timing/noise/EM fix
SRAM circuit design. Single ended, differential, dynamic, L2Tag, register file, Decoder and I/O

Hardware Engineer
Toshiba Corporation japan
Oct 1997 - May 2001 · 3 yrs 8 mos
Kawasaki, Kanagawa, Japan

Development of timing estimation and budgeting flow from floorplan.
Repeater insertion methodology and flow development.
RC extraction flow, backend verification.
Floorplan, synthesis, place and route, and timing check.
Hierarchical floorplan, place and route.

Hardware Engineer
Toshiba America Electronic Components, Inc.
Nov 1995 - Sep 1997 · 1 yr 11 mos
San Francisco Bay Area

Project with SGI/MIPS
Circuit design methodology definition.
- Noise simulation and design guidelines
- RC delay, power grid simulation and design guidelines

CAM circuit design

Hardware Engineer
Toshiba Corporation japan
Apr 1986 - Oct 1995 · 9 yrs 7 mos
Kawasaki, Kanagawa, Japan

RTL and circuit design of integer unit in CPU.
Static timing analysis, timing budgeting.
Development of architecture and gate level power estimation tool.
Standard cell library design.
Register file design.

Master's degree, Electrical, Electronics and Communications Engineering
1984 - 1986

Skills

Integrated Circuit Design

Endorsed by 4 colleagues at Oracle

4 endorsements

IC Layout

Endorsed by 4 colleagues at Oracle

4 endorsements

Standard Cell

Endorsed by 4 colleagues at Oracle

4 endorsements

Show all 8 skills →

Languages

English

Professional working proficiency

Japanese

Native or bilingual proficiency

Contact

www.linkedin.com/in/yukio-otaguro-2119a8144 (LinkedIn)

Top Skills

Integrated Circuit Design
IC Layout
Standard Cell

Languages

Japanese (Native or Bilingual)
English (Professional Working)

Yukio Otaguro

Hardware Engineer
San Jose, California, United States

Summary

-

Experience

Oracle
Hadware Engineer
February 2010 - August 2017 (7 years 7 months)
santa clara, CA

SRAM design.
EMIR, signal integrity, power, noise check and flow verification.
Standard cell library design.
CPU integration. Global clock, power grid, bump, design and physical verification.

Sun Microsystems
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May 2001 - January 2010 (8 years 9 months)
Santa clara ca

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Register file design.

Education

Tohoku University
Master's degree, Electrical, Electronics and Communications Engineering · (1984 - 1986)